AMD NPT Family 0Fh Processor Electrical Data Sheet

Publication # **31119**
Revision: **3.00**
Issue Date: **August 2006**

© 2004–2006 Advanced Micro Devices, Inc. All rights reserved.

The contents of this document are provided in connection with Advanced Micro Devices, Inc. (“AMD”) products. AMD makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. The information contained herein may be of a preliminary or advance nature and is subject to change without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in AMD’s Standard Terms and Conditions of Sale, AMD assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

AMD’s products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of AMD’s product could create a situation where personal injury, death, or severe property or environmental damage may occur. AMD reserves the right to discontinue or make changes to its products at any time without notice.

Trademarks

AMD, the AMD Arrow logo, and combinations thereof are trademarks of Advanced Micro Devices, Inc.

HyperTransport is a licensed trademark of the HyperTransport Technology Consortium.

MMX is a registered trademark of Intel Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

Contents

1 Absolute Maximum Ratings 7

2 HyperTransport™ Technology Interface 8
- 2.1 HyperTransport™ Technology Operating Conditions 8
- 2.2 HyperTransport Technology Timing Characteristics 10
- 2.3 HyperTransport Internal Termination 10
- 2.4 HyperTransport Technology Pin States During Reset and Power Management States 11

3 DDR2 SDRAM 12
- 3.1 DDR2 SDRAM Operating Conditions 12
- 3.2 DDR2 SDRAM Timing Characteristics 20
- 3.3 DDR2 SDRAM Output Pin States during Reset, S1, and S3 27

4 Miscellaneous Pins 28
- 4.1 CLKIN_H/L Pins 28
- 4.2 VID Interface Pins 29
- 4.3 Miscellaneous Input Pins 30
- 4.4 Miscellaneous Output Pins 30
- 4.5 Miscellaneous Bi-Directional Pins 31
- 4.6 Miscellaneous Pin States During Reset and Power Management States 32

5 Thermal Diode and Thermal Protection 33
- 5.1 Thermal Diode Specifications 33
- 5.2 THERMTRIP_L Thermal Protection 35

6 Power Supplies 36
- 6.1 Power Supply and PWROK Relationships 36
- 6.2 PWROK Sequencing Requirements 36
- 6.3 Power-Up (S3/S4/S5/G2 Exit) Power Sequencing Group Requirements 36
- 6.4 Powerdown (S4/S5/G2 Entry) and Power Failure (G3 Entry) Power Sequencing Group Requirements 37
- 6.5 S3 Entry Power Sequencing Group Requirements 37

7 Signal Sequencing 38
- 7.1 Power-Up Power Supply and Signal Sequencing 38

8 Internal Termination Reference Information 40

List of Figures

Figure 1. RTT = (VTT – Vx)/Ix 16
Figure 2. Output Switching 16
Figure 3. The tCKS Timing Parameter 21
Figure 4. The tDQS Timing Parameter 22
Figure 5. The tDSS and tDSH Timing Parameter 22
Figure 6. The tDQSQV and tDQSQIV Timing Parameter 23
Figure 7. The t1 Timing Parameter 24
Figure 8. The t2 Timing Parameter 24
Figure 9. The t3 Timing Parameter 25
Figure 10. The t4 Timing Parameter 26
Figure 11. CLKIN_H/L Waveform Diagram 29
Figure 12. Power-Up Power Supply and Signal Sequencing 39

List of Tables

Table 1. Revision History 6
Table 2. Absolute Maximum Ratings 7
Table 3. DC Operating Conditions for HyperTransport™ Technology Interface 8
Table 4. AC Operating Conditions for HyperTransport Technology Interface 9
Table 5. HyperTransport Technology Interface Timing Characteristics 10
Table 6. Internal Termination for HyperTransport Technology Interface 10
Table 7. HyperTransport Technology Output Pin States During Reset, S1, and S3 11
Table 8. DDR2 Pin Groups 12
Table 9. DC Operating Conditions 12
Table 10.AC Operating Conditions 14
Table 11.Input Capacitance of DDR2 SDRAM Signals 14
Table 12.Output Slew Rate of DDR2 SDRAM Signals 14
Table 13.Input Slew Rate of DDR2 SDRAM Signals 15
Table 14.M*_DATA*, M*_DQS_*, M*_DM*, M*_CHECK*, M*_CLK_*
Driver Characteristics 1.0x 18
Table 15.Address, Command, Control and Data Driver Characteristics 1.5x 19
Table 16.Address, Command and Control Driver Characteristics 2.0x 20
Table 17.Electrical AC Timing Characteristics 20
Table 18.DDR2 SDRAM Output Pin States During Reset, S1, and S3 27
Table 19.Operating Conditions for CLKIN_H/L 28
Table 20.Combined AC and DC Operating Conditions for VID[5:0], and PSI_L 29
Table 21.Combined AC and DC Operating Conditions for RESET_L, LDTSTOP_L,
and PWROK 30
Table 22.Combined AC and DC Operating Conditions for TCK, TDI, TMS, TRST_L,
and DBREQ_L 30
Table 23.Combined AC and DC Operating Conditions for TDO, DBRDY 30
Table 24.Combined AC and DC Operating Conditions for THERMTRIP_L 31
Table 25.Combined AC and DC Operating Conditions for PROCHOT_L 31
Table 26.Miscellaneous Output Pin States During Reset, S1, and S3 32
Table 27.Miscellaneous Input Pin Requirements During Reset, S1, and S3 32
Table 28.Thermal Diode Specifications for Socket F (1207) and
Socket AM2 Processors 33
Table 29.Thermal Diode Specifications for Socket S1g1 Processors 34
Table 30.Platform Thermal Protection Limits for the Processor 35
Table 31.Power Sequencing Group Definitions 36
Table 32.Internal Termination for Miscellaneous Pins Interface and Test Pins 40

Table 1. Revision History

Date	Revision	Description
August 2006	3.00	Initial public release.

1 Absolute Maximum Ratings

Stresses greater than those listed in Table 2 may cause permanent damage to the device and motherboard. Systems using this device must be designed to ensure that these parameters are not violated. Violation of these ratings voids the product warranty. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Characteristic	Range
Storage Temperature	–55ºC to 85ºC
VLDT supply voltage relative to VSS	–0.3 V to 1.5 V
VDD supply voltage relative to VSS	–0.3 V to 1.65 V
VTT supply voltage relative to VSS	–0.3 V to 1.1 V (see Note 1)
VDDIO supply voltage relative to VSS	–0.3 V to 2.2 V (see Note 1)
VDDA supply voltage relative to VSS	–0.3 V to 3.0 V
M_V_{REF} input voltage relative to VSS	–0.3 V to VDDIO + 0.3 V
Input voltage relative to VSS for HyperTransport™ technology interface	–0.3 V to VLDT + 0.3 V
Differential input voltage for HyperTransport technology interface	–1.5 V to 1.5 V
Input voltage relative to VSS for DDR2 SDRAM memory interface and Miscellaneous pins	–0.3 V to VDDIO + 0.3 V (see Note 2)

Notes:

1.See “Power Supply and PWROK Relationships” on page 36 for the relationship between VDDIO and VTT.

2.The input voltage of these pins can momentarily go to –1.0 V during capacitor charging prior to PWROK assertion. In Section 3, see the various operating condition tables on DDR2 pins and Miscellaneous pins for the relationship between these pins and VDDIO.

2 HyperTransport™ Technology Interface

2.1 HyperTransport™ Technology Operating Conditions

Table 3. DC Operating Conditions for HyperTransport™ Technology Interface

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{OD}	Output differential voltage	mV	495	600	715	1, 2
V_{OCM}	Output common mode voltage	mV	495	600	715	1, 2
VID	Input differential voltage	mV	100	600	1000	1, 2
V_{ICM}	Input common mode voltage	mV	440	600	780	1, 2
DeltaV_{OD}	Change in V_{OD} from 0 to 1 state	mV	–15	0	15	1
DeltaV_{OCM}	Change in V_{OCM} from 0 to 1 state	mV	–15	0	15	1
DeltaVID	Change in VID from 0 to 1 state	mV	–15	0	15	1
DeltaV_{ICM}	Change in V_{ICM} from 0 to 1 state	mV	–15	0	15	1
I_I	Input leakage current	µA	–500		500	
I_{OZ}	Output tristate leakage current	mA	–1		1	
RTT	Input differential impedance	Ohm	90	100	110	
R_{ON}	Output driver impedance	Ohm	45	50	55	
DeltaR_{ON}	Change in R_{ON} driving 0=>1 or 1=>0	%	0	0	5	

Notes:

1. *Measured by comparing each signal voltage with respect to ground.*
2. *Measured at <100 MHz, considered slow enough to attain both 0 and 1 logic state voltage levels without AC transients on signals and supplies.*

Table 4. AC Operating Conditions for HyperTransport™ Technology Interface

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{OD}	Output differential voltage	mV	400	600	820	1
V_{OCM}	Output common mode voltage	mV	440	600	780	1
VID	Input differential voltage	mV	200	600	900	1, 3
V_{ICMAC}	Peak-to-peak magnitude of input common mode voltage	mV			350	1, 3
$DeltaV_{OD}$	Change in V_{OD} from 0 to 1 State	mV	–75		75	1
$DeltaV_{OCM}$	Change in V_{OCM} from 0 to 1 State	mV	–50		50	1
DeltaVID	Change in VID from 0 to 1 State	mV	–125		125	1
T_{IR}	Input rising slew rate	V/ns	2.0		8.0	2, 3
T_{IF}	Input falling slew rate	V/ns	2.0		8.0	2, 3
T_{OR}	Output rising slew rate	V/ns	2.5		8.0	4
T_{OF}	Output falling slew rate	V/ns	2.5		8.0	4
C_{IN}	Input pad capacitance, 600 MHz, 800 MHz, 1.0 GHz	pF			2	5
C_{OUT}	Output pad capacitance, 600 MHz, 800 MHz, 1.0 GHz	pF			3	5
C_{DELTA}	C_{IN} pad capacitance range across group	pF			0.5	

Notes:

1. *Measured by comparing each signal voltage with respect to ground.*
2. *Measured differentially between ±100 mV.*
3. *Only simulated at the receive die pad. This parameter is intended to give guidance for simulation. It is guaranteed by design and cannot be tested on a tester.*
4. *Output slew rates are measured differentially between ±200 mV.*
5. *C_{IN} and C_{OUT} are measured with a time domain reflectometer (TDR) set to a low repeat rate or equivalent measurement technique.*

2.2 HyperTransport™ Technology Timing Characteristics

Table 5. HyperTransport™ Technology Interface Timing Characteristics

Symbol	Parameter	Unit	Min	Typ	Max	Notes
T_{CADV}	Transmitter output CAD/CTLOUT valid relative to CLKOUT, 200 MHz	ps	695			1, 5
	Transmitter output CAD/CTLOUT valid relative to CLKOUT, 400 MHz	ps	345			1, 5
	Transmitter output CAD/CTLOUT valid relative to CLKOUT, 600 MHz	ps	234			1, 5
	Transmitter output CAD/CTLOUT valid relative to CLKOUT, 800 MHz	ps	166			1, 5
	Transmitter output CAD/CTLOUT valid relative to CLKOUT, 1.0 GHz	ps	183			1, 4, 5
T_{CADVRS}	Receiver input CADIN valid time to CLKIN	ps	92			1, 3
T_{CADVRH}	Receiver input CADIN valid time from CLKIN	ps	105			1, 3
T_{PHERR}	Accumulated phase error, CLKIN_H/L to L*_CLKOUT_H/L[1:0]	ps	0		5000	
T_{SU}	Device setup time	ps			85	1, 2
T_{HLD}	Device hold time	ps			98	1, 2

Notes:

1. *All timing measurement points are at the zero crossing points of differential pairs.*
2. *Only simulated at the receive die pad. This parameter is intended to give guidance for data bus simulation. It is guaranteed by design and cannot be tested on a tester.*
3. *Measured at the receiver pins.*
4. *T_{CADV} of 183 ps for 1000 MHz operation implies a maximum TX CAD to CLK skew of 67 ps at the device pins. Refer to the* HyperTransport™ I/O Link Specification *for further details.*
5. *Measured at the transmitter pins into the ideal test load described in the* HyperTransport™ I/O Link Specification.

2.3 HyperTransport™ Internal Termination

Table 6. Internal Termination for HyperTransport™ Technology Interface

Pin	Internal Termination	Value	Tolerance
L*_CADIN*	Differential RTT	100 ohms (PVT-compensated)	±10%
L*_CTLIN*	Differential RTT	100 ohms (PVT-compensated)	±10%
L*_CLKIN*	Differential RTT	100 ohms (PVT-compensated)	±10%

2.4 HyperTransport™ Technology Pin States During Reset and Power Management States

The default pin states for HyperTransport™ Technology output pins during reset and ACPI power management states are listed in Table 7. Chapter 7, on page 38, contains additional information and requirements for signal sequencing for certain input and output pins.

Table 7. HyperTransport™ Technology Output Pin States During Reset, S1, and S3†

Pin Name	Reset	S1	S3	Comments
L*_CLKOUT*	T	Z	Z	Tristated in S1 only if programmed to do so.
L*_CTLOUT*	0	Z	Z	Tristated in S1 only if programmed to do so.
L*_CADOUT*	1	Z	Z	Tristated in S1 only if programmed to do so.

†Notes:

- *For differential pins "0" and "1" refer to the high-end differential output. Low-end differential outputs are inverted.*
- *Definition of pin states:*
    - *X—Either logic 1 or logic 0.*
    - *Z—Tristated.*
    - *T—Toggling between 0 and 1.*

3 DDR2 SDRAM

3.1 DDR2 SDRAM Operating Conditions

In this chapter, some DDR2 pins are grouped together and given group names. The groups are defined in the following Table 8.

Table 8. DDR2 Pin Groups

Pin group names	Pins
Address	M*_ADD*, M*_BANK*
Command	M*_RAS_L, M*_CAS_L, M*_WE_L, M*_PAR
Control	M*_CS_L, M*_ODT and M*_CKE*
Data	M*_DATA*, M*_DQS*, M*_DM*, M*_CHECK*, M*_CLK*

The notes for Table 9 through Table 13 on page 15 begin on page 15.

Table 9. DC Operating Conditions

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{REF}	Reference voltage (for I/O)	V	0.49* VDDIO_dc	0.50* VDDIO_dc	0.51* VDDIO_dc	2
VTT	Termination voltage (for I/O)	V	0.50* VDDIO_dc	0.50* VDDIO_dc	0.50* VDDIO_dc	2
I_l	Input leakage current Any input: $0 \le V_{IN} \le$ VDDIO V (All other pins not under test = 0 V)	mA	–1		1	1
I_{oz}	Output leakage current Any output: $0 \le V_{OUT} \le$ VDDIO V	mA	–1		1	1
V_{IH}	Input high voltage (logic 1)	V	V_{REF} + 0.125	–	–	3
V_{IL}	Input low voltage (logic 0)	V	–	–	V_{REF} – 0.125	3
V_{OH}	Output high voltage (logic 1) for Data and M*_RESET_L pins (1x drive strength)	V	1.34 (1.18)			20, 24
V_{OL}	Output low voltage (logic 0) for Data and M*_RESET_L pins (1x drive strength)	V			0.38 (0.53)	20, 24
I_{OH}	Output levels -Output high current for Data and M*_RESET_L pins (V_{OUT}= VDDIO/2) (1x drive strength)	mA	–19.0	–22.5	–29.5	4, 24

Table 9. DC Operating Conditions (Continued)

Symbol	Parameter	Unit	Min	Typ	Max	Notes
I_{OL}	Output levels - Output low current for Data and M*_RESET_L pins (V_{OUT}=VDDIO/2) (1x drive strength)	mA	19.0	22.5	28.0	4, 24
V_{OH}	Output high voltage (Logic 1) for Address, Command, Control, Data and M*_RESET_L pins (1.5x drive strength)	V	1.40 (1.26)			20, 25, 28
V_{OL}	Output low voltage (Logic 0) for Address, Command, Control, Data and M*_RESET_L pins (1.5x drive strength)	V			0.30 (0.46)	20, 25, 28
I_{OH}	Output levels – Output high current for Address, Command, Control, Data and M*_RESET_L pins (V_{OUT}= VDDIO/2) (1.5x drive strength)	mA	–27.0	–34.0	–45.0	4, 25, 28
I_{OL}	Output levels – Output low current for Address, Command, Control, Data and M*_RESET_L pins (V_{OUT}= VDDIO/2) (1.5x drive strength)	mA	27.5	33.5	42.0	4, 25, 28
V_{OH}	Output high voltage (logic 1) for Address, Command, and Control pins (2.0x drive strength)	V	1.45 (1.32)			20, 26, 28
V_{OL}	Output low voltage (logic 0) for Address, Command and Control pins (2.0x drive strength)	V			0.25 (0.38)	20, 26, 28
I_{OH}	Output levels – Output high current for Address, Command and Control pins (V_{OUT}= VDDIO/2) (2.0x drive strength)	mA	–37.0	–45.0	–61.0	4, 26, 28
I_{OL}	Output levels – Output low current for Address, Command and Control pins (V_{OUT}= VDDIO/2) (2.0x drive strength)	mA	37.0	45.0	57.0	4, 26, 28
VID	Differential Input voltage (for M*_DQS_*)	V	0.25	-	-	5
Delta VID	Change in VID magnitude	mV	–200	-	200	6
Delta V_{Swing}	Difference in voltage swing between M*_DQS_* and associated M*_DATA*	mV	–300	0	300	22
V_{ICM}	Input common mode voltage (for M*_DQS_*)	V	0.7	0.9	1.1	7
V_{OD}	Differential output voltage (for M*_CLK_* and M*_DQS_*)	V	1.18 (0.87)	-	-	9, 20

Table 9. DC Operating Conditions (Continued)

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{OCM}	Output common mode voltage (for M*_CLK_* and M*_DQS_*)	V	0.75	0.9	1.05	11, 20
RTT	On-die termination	Ohm		75 or 150 or 300		13

Table 10. AC Operating Conditions

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{REF}	Reference voltage (for I/O)	V	V_{REF}(DC) – 2%		V_{REF}(DC) + 2%	2
VTT	Termination voltage (for I/O)	V	V_{REF}(DC) – 0.075		V_{REF}(DC) + 0.075	2
V_{IH}	Input high voltage (logic 1)	V	V_{REF} + 0.2	–	VDDIO + 0.15	3
V_{IL}	Input low voltage (logic 0)	V	– 0.15	–	V_{REF} – 0.2	3
VID	Differential input voltage (for M*_DQS_*)	V	0.5	–	VDDIO + 0.3	5
Delta VID	Change in VID magnitude	mV	–400		400	6
V_{IX}	Input crosspoint voltage	mV	0.5* VDDIO_dc – 250	0.5* VDDIO_dc	0.5* VDDIO_dc + 250	21
Delta V_{ICM}	Change in V_{ICM} magnitude	mV	–50	–	50	8
Delta V_{OCM}	Change in V_{OCM} magnitude	mV	–30	–	30	12, 20
V_{OX}	Output crosspoint voltage	mV	0.5* VDDIO_dc – 125	0.5* VDDIO_dc	0.5* VDDIO_dc + 125	23, 20

Table 11. Input Capacitance of DDR2 SDRAM Signals

Symbol	Parameter	Unit	Min	Typ	Max	Notes
C_{in}	Input capacitance (M*_DATA*, M*_DQS_*,)	pF	1.3	1.8	2.3	27
Delta C	Delta input capacitance	pF	–	–	0.4	14

Table 12. Output Slew Rate of DDR2 SDRAM Signals

Symbol	Parameter	Unit	Min	Typ	Max	Notes
S_{OUT}	Output slew rate (pullup and pulldown) – 1.0x Drive Strength	V/ns	2	5	10	15

Table 12. Output Slew Rate of DDR2 SDRAM Signals (Continued)

Symbol	Parameter	Unit	Min	Typ	Max	Notes
S_{OUT}	Output slew rate (pullup and pulldown) – 1.5x Drive Strength	V/ns	2		12	15
S_{OUT}	Output slew rate (pullup and pulldown) – 2.0x Drive Strength	V/ns	2		12	15
S_{OUT_Ratio}	Output slew rate ratio between pullup and pulldown – 1.0x, 1.5x and 2.0x Drive Strength		0.75	1	1.25	16

Table 13. Input Slew Rate of DDR2 SDRAM Signals

Symbol	Parameter	Unit	400 MT/s		533 MT/s		667 MT/s		800 MT/s		Notes
			Min	Max	Min	Max	Min	Max	Min	Max	
S_{in}	Input slew rate — single-ended signals	V/ns	0.5	2.5	0.5	2.5	0.5	2.5	0.5	2.5	17
S_{in}	Input slew rate — differential signals	V/ns	1	5	1.0	5	1.0	5	1.0	5	17
$S_{mismatch}$	Input slew rate mismatch between M*_DQS_* and associated M*_DATA*/M*_CHECK*	V/ns	–0.2	0.2	–0.2	0.2	–0.2	0.2	–0.5	0.5	18
$S_{mismatch}$	Input slew rate mismatch between M*_DQS_* and associated M*_DATA*/M*_CHECK*	V/ns	–0.5	0.5	–0.5	0.5	–0.5	0.5	N/A		19

Notes:

1. *Leakage current is measured when the pin is configured to high-impedance state and with all on-die termination disabled.*
2. *V_{REF} and VTT are expected to be equal to 0.5*VDDIO and to track variations in the DC level of the same.*
3. *The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. The receiver effectively switches to the new logic state when receiver input crosses the AC level. The new logic state is maintained as long as the input stays beyond the DC threshold.*
4. *Table 14 on page 18, Table 15 on page 19, and Table 16 on page 20 show the pullup and pulldown driver characteristics.*

    Typical: 25º C ($T_{Ambient}$), VDDIO_dc=1.8 V, Typical process

    Minimum: 70º C ($T_{Ambient}$), VDDIO_dc=1.7 V, Slow-slow process

    Maximum: 0º C ($T_{Ambient}$), VDDIO_dc=1.9 V, Fast-fast process
5. *VID is the input differential voltage or the voltage difference between the true and complement under DC or AC conditions.*

6. *Delta VID is the change in magnitude between the input differential voltage while receiving a Logic 0 and while receiving a Logic 1. Delta VID represents the change in magnitude from one bit time to next bit time.*
7. *V_{ICM} is the input common mode voltage defined as the average of the true voltage magnitude and the complement voltage magnitude relative to ground under DC conditions. This parameter includes the variation due to power supply.*
8. *Delta V_{ICM} is the change in magnitude between the input common mode voltage while receiving a Logic 0 and while receiving a Logic 1. Delta V_{ICM} represents the variation in input common mode voltage from one bit time to next bit time.*
9. *V_{OD} is the differential output voltage or the voltage difference between true and complement under DC or AC conditions.*
10. *Delta V_{OD} is the change in magnitude between the differential output voltage while driving a Logic 0 and while driving a Logic 1.*
11. *V_{OCM} is the output common mode voltage defined as the average of the true voltage magnitude and the complement voltage magnitude relative to ground under DC or AC conditions.*
12. *Delta V_{OCM} is the change in magnitude between the output common mode voltage while driving a Logic 0 and while driving a Logic 1.*
13. *The RTT value is programmable depending on system configuration. The tolerance for each value is 20%. This termination applies to all M*_DATA*, M*_DQS_* when enabled. This specification is guaranteed by design and characterization only. To characterize, apply some voltage V_x at the pin and measure the current I_x. RTT = $(VTT - V_x)/I_x$.*

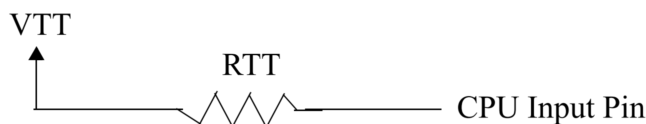

Figure 1. **RTT = $(VTT - V_x)/I_x$**

14. *Delta C means the difference in capacitance between any M*_DATA*/DQS_* pin to any other M*_DATA*/DQS_* pin.*
15. *Pullup and pulldown slew rate is measured into RTT (50 ohms) to VTT. The slew rate is measured between $V_{REF} \pm 250$ mV. It is guaranteed for any pattern of data, including all outputs switching and only one output switching.*

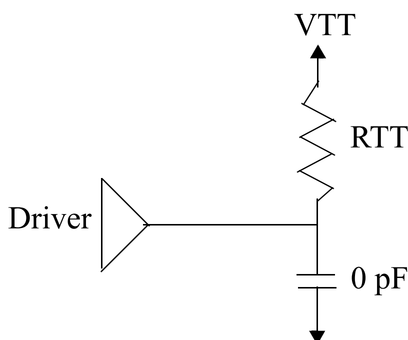

Figure 2. **Output Switching**

16. *The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.*
17. *The slew rate is measured at the CPU pin between $V_{REF} \pm 125$ mV for single-ended signals. For differential input signal, the slew rate is measured differentially at the CPU pin between $\pm$ 250 mV. The single-ended input slew rate parameter also applies to the M*_ERR_L pin.*
18. *When nominal slew rate of an input signal (M*_DQS_* or its associated M*_DATA*) is 1.5 V/ns or less at the processor pin, then the slew rate mismatch between M*_DQS_* and its associated M*_DATA* is maximum of $\pm$ 200 mV/ns from the nominal slew rate.*
19. *When nominal slew rate of an input signal (M*_DQS_* or its associated M*_DATA*) is 1.5 V/ns or higher at the processor pin, then the slew rate mismatch between M*_DQS_* and its associated M*_DATA* is maximum of $\pm$ 500 mV/ns from the nominal slew rate. The absolute highest slew rate at processor pin is 2.5 V/ns.*
20. *The values are defined assuming that output test load is 50 ohms to VTT. The value in parentheses is for output test load assuming 25 ohms to VTT .*
21. *The typical value of V_{IX} is expected to be 0.5*VDDIO of the transmitting device and is expected to track variations in VDDIO. V_{IX} indicates the voltage at which differential input signals must cross over one bit time to any other bit time. V_{IX} consists of input slew rate mismatch, trace mismatch between differential signals, input capacitive mismatch, crosstalk noise, etc.*
22. *During a given bit time, Delta V_{Swing} is the difference in voltage swing between M*_DQS_* and associated M*_DATA*. The voltage swing for M*_DQS_H* and M*_DQS_L* is measured single-ended.*
23. *The typical value of V_{OX} is expected to be 0.5*VDDIO of the transmitting device and is expected to track variations in VDDIO. V_{OX} indicates the voltage at which differential output signals must cross over one bit time to any other bit time. V_{OX} consists of output slew rate mismatch, package trace mismatch between differential signals, crosstalk noise, etc.*
24. *The specification assumes nominal drive strength of 40 ohms. If drive strength is adjusted, the specification also changes.*
25. *The specification assumes nominal drive strength of 27 ohms. If drive strength is adjusted, the specification also changes.*
26. *The specification assumes nominal drive strength of 20 ohms. If drive strength is adjusted, the specification also changes.*
27. *This parameter is measured at the “pad” and not at the package pin. The “pad” capacitance includes all parasitics capacitance from the pad silicon, through the C4 plus package landing pad and via to the start of the package trace. This is guaranteed by design and verification.*
28. *These parameters are generated based on the specification of the memory controller pins only, and it does not represent the actual system loading environment.*

Table 14. M*_DATA*, M*_DQS_*, M*_DM*, M*_CHECK*, M*_CLK_* Driver Characteristics 1.0x

	Pulldown Current (mA)			Pullup Current (mA)		
Voltage	**Minimum**	**Typical**	**Maximum**	**Minimum**	**Typical**	**Maximum**
0	0.0	0.0	0.0	–26.2	–33.0	–42.9
0.1	2.6	3.0	3.7	–25.5	–32.0	–41.5
0.2	5.2	6.0	7.3	–24.8	–31.0	–40.1
0.3	7.7	9.0	10.8	–24.1	–29.8	–38.6
0.4	10.2	11.8	14.2	–23.4	–28.6	–37.2
0.5	12.5	14.4	17.5	–22.6	–27.4	–35.8
0.6	14.7	16.9	20.5	–21.7	–26.2	–34.3
0.7	16.6	19.2	23.2	–20.7	–25.0	–32.9
0.8	18.2	21.0	25.4	–19.6	–23.8	–31.5
0.9	19.5	22.5	27.2	–18.2	–22.5	–30.0
1.0	20.5	23.7	28.6	–16.5	–20.9	–28.6
1.1	21.3	24.9	30.1	–14.5	–18.9	–27.0
1.2	22.1	26.0	31.5	–12.4	–16.7	–25.0
1.3	22.9	27.0	33.0	–10.1	–14.3	–22.7
1.4	23.7	28.0	34.4	–7.7	–11.6	–20.0
1.5	24.3	29.0	35.8	–5.2	–8.9	–17.1
1.6	24.9	30.0	37.3	–2.6	–6.0	–13.9
1.7	25.5	31.0	38.7	0.0	–3.0	–10.6
1.8		32.0	40.0		0.0	–7.2
1.9			41.2			–3.6

Table 15. Address, Command, Control and Data Driver Characteristics 1.5x

	Pulldown Current (mA)			Pullup Current (mA)		
Voltage	**Minimum**	**Typical**	**Maximum**	**Minimum**	**Typical**	**Maximum**
0	0.0	0.0	0.0	–38.0	–49.5	–64.2
0.1	3.8	4.6	5.6	–37.0	–48.7	–62.2
0.2	7.6	9.1	11.1	–36.0	–46.3	–60.2
0.3	11.3	13.4	16.5	–35.0	–44.7	–58.1
0.4	14.8	17.7	21.6	–33.9	–42.9	–56.1
0.5	18.2	21.7	26.6	–32.7	–41.1	–54.0
0.6	21.3	25.4	31.1	–31.5	–39.3	–52.0
0.7	24.1	28.7	35.2	–30.0	–37.5	–49.9
0.8	26.5	31.6	38.7	–28.4	–35.7	–47.9
0.9	28.3	33.8	41.4	–26.3	–33.8	–45.7
1.0	29.7	35.4	43.5	–23.9	–31.3	–43.5
1.1	31.0	37.0	45.5	–21.1	–28.4	–41.1
1.2	32.2	38.6	47.6	–18.0	–25.1	–38.1
1.3	33.3	40.2	49.7	–14.7	–21.4	–34.6
1.4	34.4	41.8	51.7	–11.2	–17.5	–30.5
1.5	35.3	43.4	53.8	–7.6	–13.3	–26.0
1.6	36.2	45.0	55.8	–3.8	–9.0	–21.3
1.7	37.0	46.6	57.7	0.0	–4.6	–16.2
1.8		48.2	59.5		0.0	–11.0
1.9			61.4			–5.5

Table 16. Address, Command and Control Driver Characteristics 2.0x

	Pulldown Current (mA)			Pullup Current (mA)		
Voltage	**Minimum**	**Typical**	**Maximum**	**Minimum**	**Typical**	**Maximum**
0	0.0	0.0	0.0	–51.2	–66.0	–86.7
0.1	5.2	6.1	7.6	–49.9	–63.8	–84.1
0.2	10.3	12.1	15.1	–48.6	–61.6	–81.4
0.3	15.2	17.9	22.3	–47.2	–59.4	–78.7
0.4	20.0	23.5	29.3	–45.7	–57.2	–76.1
0.5	24.5	28.9	35.9	–44.1	–54.8	–73.2
0.6	28.7	33.9	42.1	–42.4	–52.4	–70.3
0.7	32.5	38.3	47.7	–40.5	–50.0	–67.4
0.8	35.6	42.1	52.3	–38.3	–47.6	–64.6
0.9	38.1	45.0	56.0	–35.5	–45.0	–61.7
1.0	40.1	47.3	58.8	–32.2	–41.8	–58.8
1.1	41.7	49.5	61.5	–28.4	–37.9	–55.6
1.2	43.3	51.7	64.1	–24.3	–33.4	–51.6
1.3	44.9	53.9	66.8	–19.8	–28.5	–46.8
1.4	46.3	56.0	69.5	–15.1	–23.3	–41.3
1.5	47.6	58.0	72.2	–10.2	–17.7	–35.2
1.6	48.8	60.0	74.8	–5.2	–12.0	–28.7
1.7	49.8	62.0	77.4	0.0	–6.1	–21.9
1.8		64.0	79.9		0.0	–14.8
1.9			82.3			–7.5

3.2 DDR2 SDRAM Timing Characteristics

Table 17. Electrical AC Timing Characteristics

Symbol	Parameter	Unit	Min	Typ	Max	Notes
tCK	M*_CLK_* cycle time	ps	2500		10000	17
tCH	M*_CLK_* high pulse width	ps	0.47*tCK		0.53*tCK	
tCL	M*_CLK_* low pulse width	ps	0.47*tCK		0.53*tCK	
tCKS	M*_CLK_* output skew	ps			225	1,2,3
tDQSH	M*_DQS_* high pulse width	ps	0.45*tCK		0.55*tCK	1
tDQSL	M*_DQS_* low pulse width	ps	0.45*tCK		0.55*tCK	1
tDQS	M*_CLK_* to M*_DQS_*	ps			225	1,4,5

Table 17. Electrical AC Timing Characteristics (Continued)

Symbol	Parameter	Unit	Min	Typ	Max	Notes
tDSS	M*_DQS_* falling edge to M*_CLK_* rising edge	ps	0.45*tCK – 250			1,6,7
tDSH	M*_CLK_* rising edge to M*_DQS_* falling edge	ps	0.45*tCK – 250			1,6,7
tDQSQV	M*_DQS_* to M*_DATA* shift (when data becomes valid)	ps	–{tCK/4 + 225}	tCK/4	–{tCK/4 – 225}	1,8,9
tDQSQIV	M*_DQS_* to M*_DATA* shift (when data becomes in-valid)	ps	{tCK/4 – 225}	tCK/4	{tCK/4 + 225}	1,8,9
t1	M*_ADD/CMD to M*_CLK_* (Unbuffered DIMM environment - M*_ADD/CMD are launched 1 clock early)	ps			225	1,10, 11
t2	M*_ADD/CMD to M*_CLK_* (unbuffered DIMM environment - M*_ADD/CMD are launched 3/4 clock early)	ps			225	1,10, 12
t3	M*_ADD/CMD to M*_CLK_* (Registered DIMM environment - M*_ADD/CMD are launched 1/2 clock early)	ps			225	1,10, 13
t4	M*_DATA* edge arrival relative to M*_DQS_*	ps	–{tCK/4 – 210}		{tCK/4 – 210}	14,15,16

Notes:

1. *Write cycle timing parameter.*
2. *The skew consists of pad skew and package routing skew between any two clock pairs.*
3. *Figure 3 shows the tCKS timing parameter:*

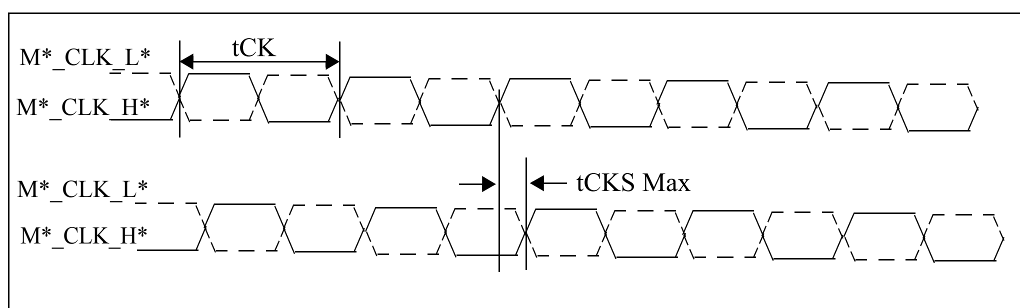

Figure 3. The tCKS Timing Parameter

4. *The timing consists of pad skew and package routing skew between any clock and any M*_DQS_* pair.*

5. *Figure 4 shows the tDQS timing parameter*:

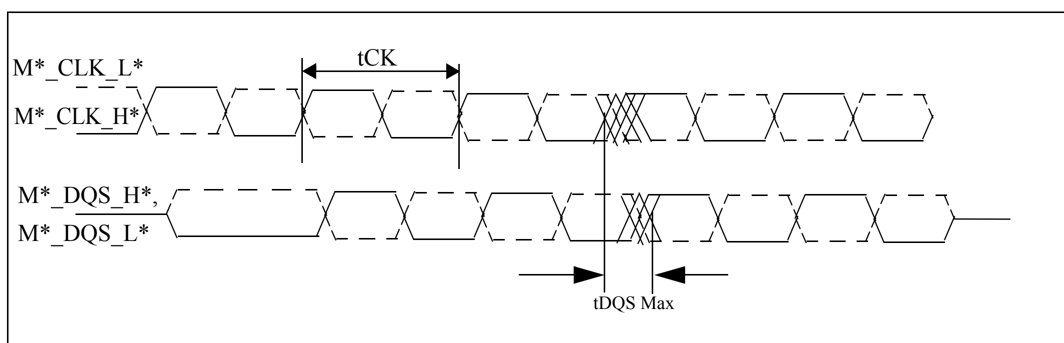

Figure 4. The tDQS Timing Parameter

6. *The skew consists of pad output skew and package routing skew between any clock pair to any M*_DQS_* pair.*
7. *Figure 5 shows the tDSS and tDSH timing parameter:*

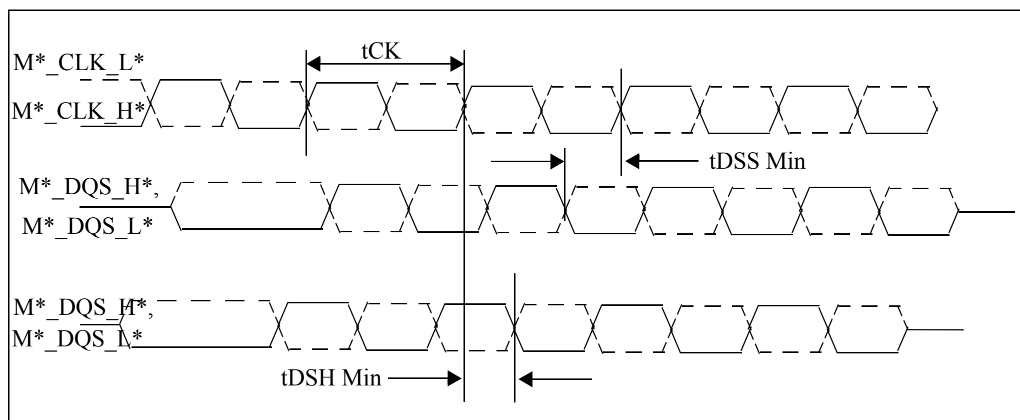

Figure 5. The tDSS and tDSH Timing Parameter

8. *During write, M*_DATA* signals are driven quarter clock earlier such that M*_DQS_* is placed in the center of data eye window. The skew consists of pad skew, package routing skew between any M*_DQS_* signals and its associated M*_DATA* signals (within a byte or nibble) and maximum clock granularity.*
9. *Figure 6 on page 23 shows the tDQSQV and tDQSQIV timing parameter. This timing parameter applies only within M*_DQS_* and its associated M*_DATA* signals.*

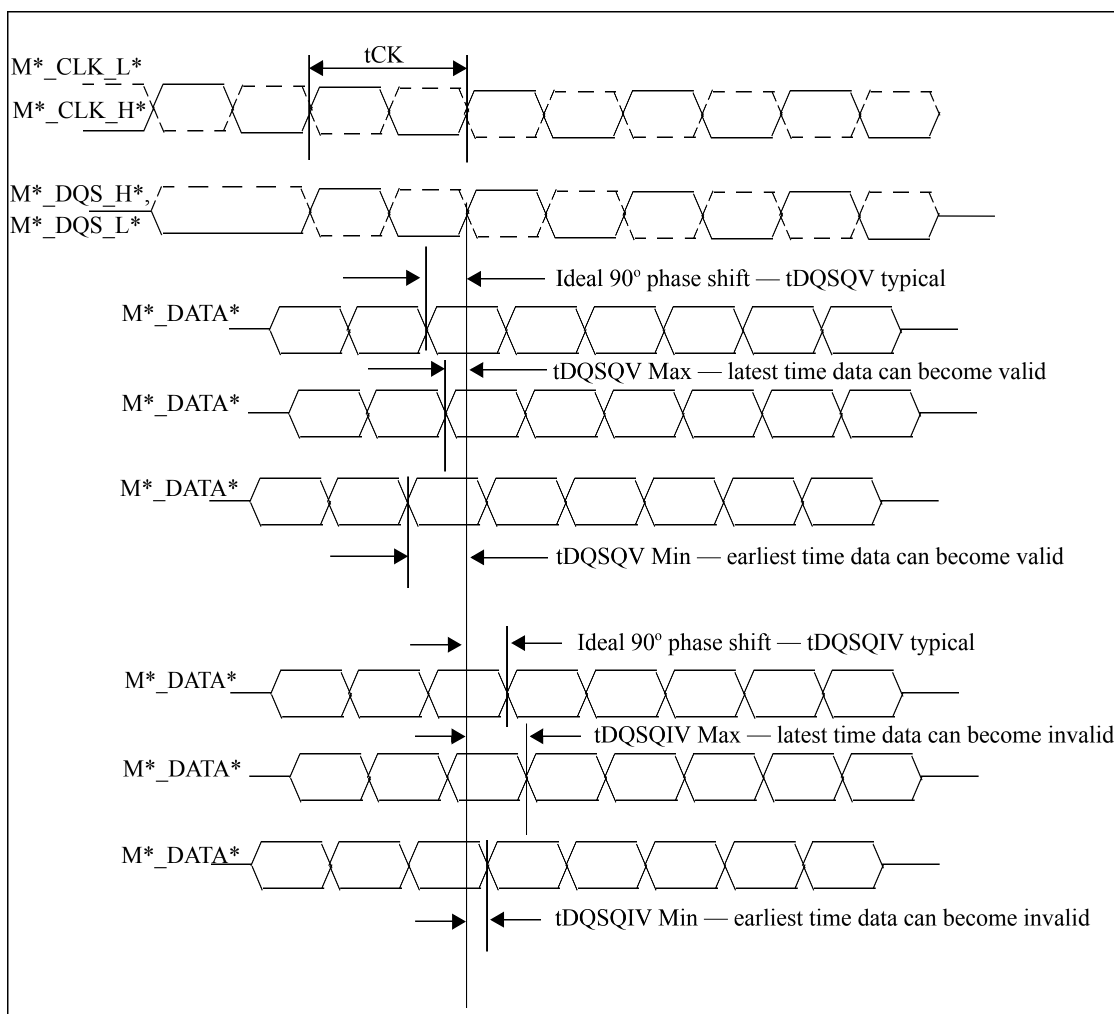

Figure 6. The tDQSQV and tDQSQIV Timing Parameter

10. *The skew consists of pad output skew and package routing skew between any clock pair to any M*_ADD/CMD/CTRL signals.*
11. *Figure 7 on page 24 shows the t1 timing parameter (unbuffered DIMM environment only). The M*_ADD/CMD signals are launched 1 clock early.*

.

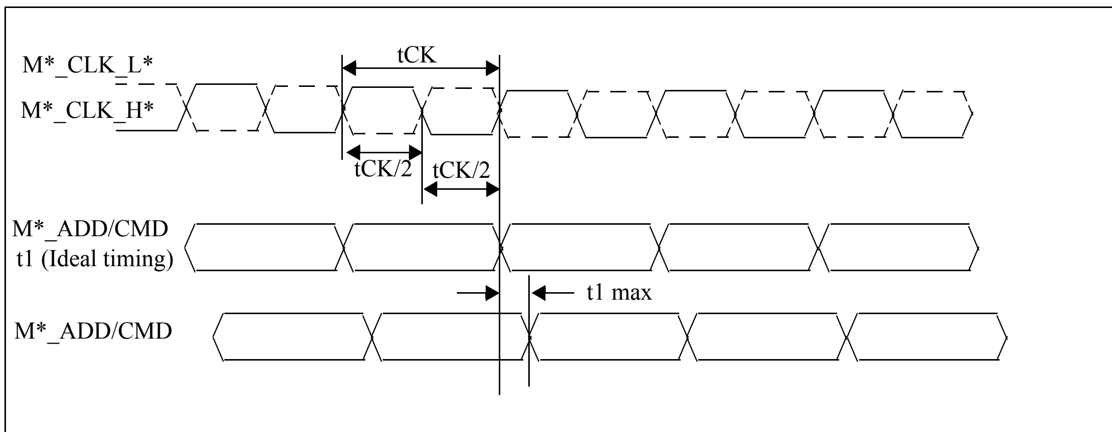

Figure 7. The t1 Timing Parameter

12. *Figure 8 shows the t2 timing parameter (unbuffered DIMM environment only). The M*_ADD/CMD signals are launched 3/4 clock early. The granularity term is included in this parameter only.*

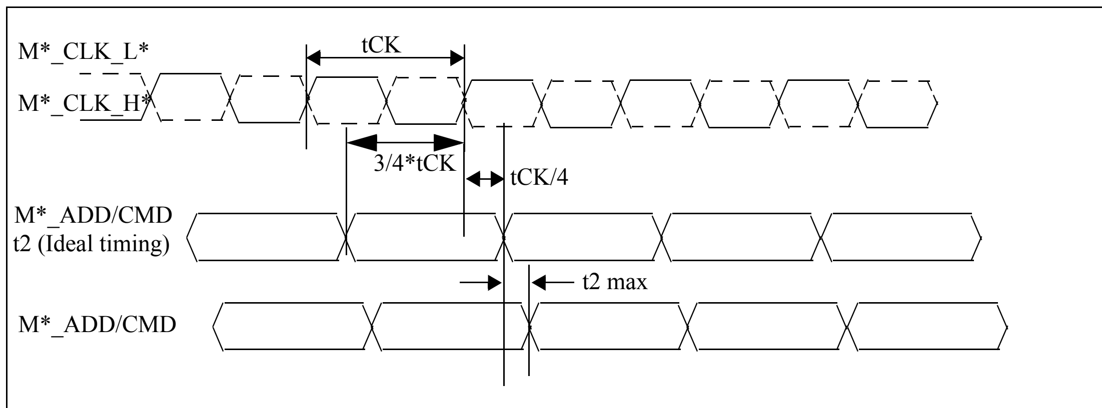

Figure 8. The t2 Timing Parameter

13. *Figure 9 on page 25 shows the t3 timing parameter (registered DIMM environment only). The M*_ADD/CMD signals are launched 1/2 clock cycle early.*

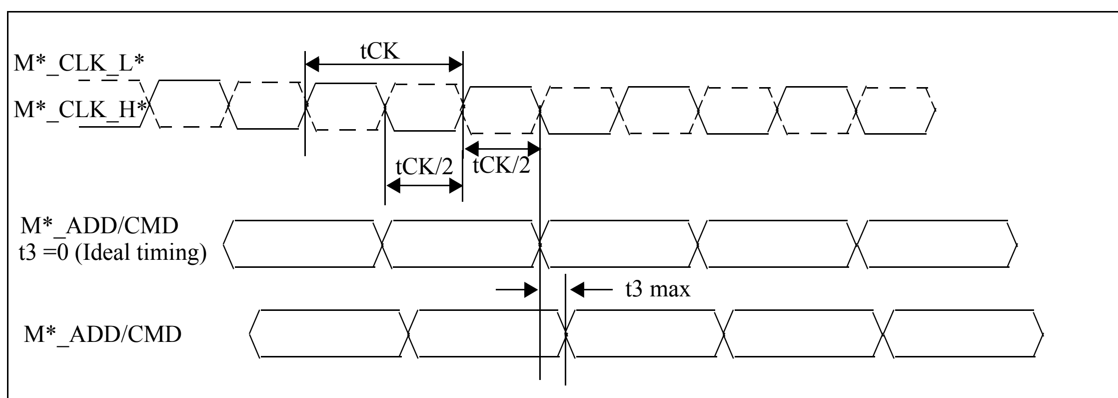

Figure 9. The t3 Timing Parameter

14. *Read cycle timing parameter.*
15. *The sum of all uncertainty contains PDL placement uncertainty, package routing skew mismatch, setup and hold time of the flop and the receiver uncertainty.*
16. *Figure 10 on page 26 shows the t4 timing parameter.*

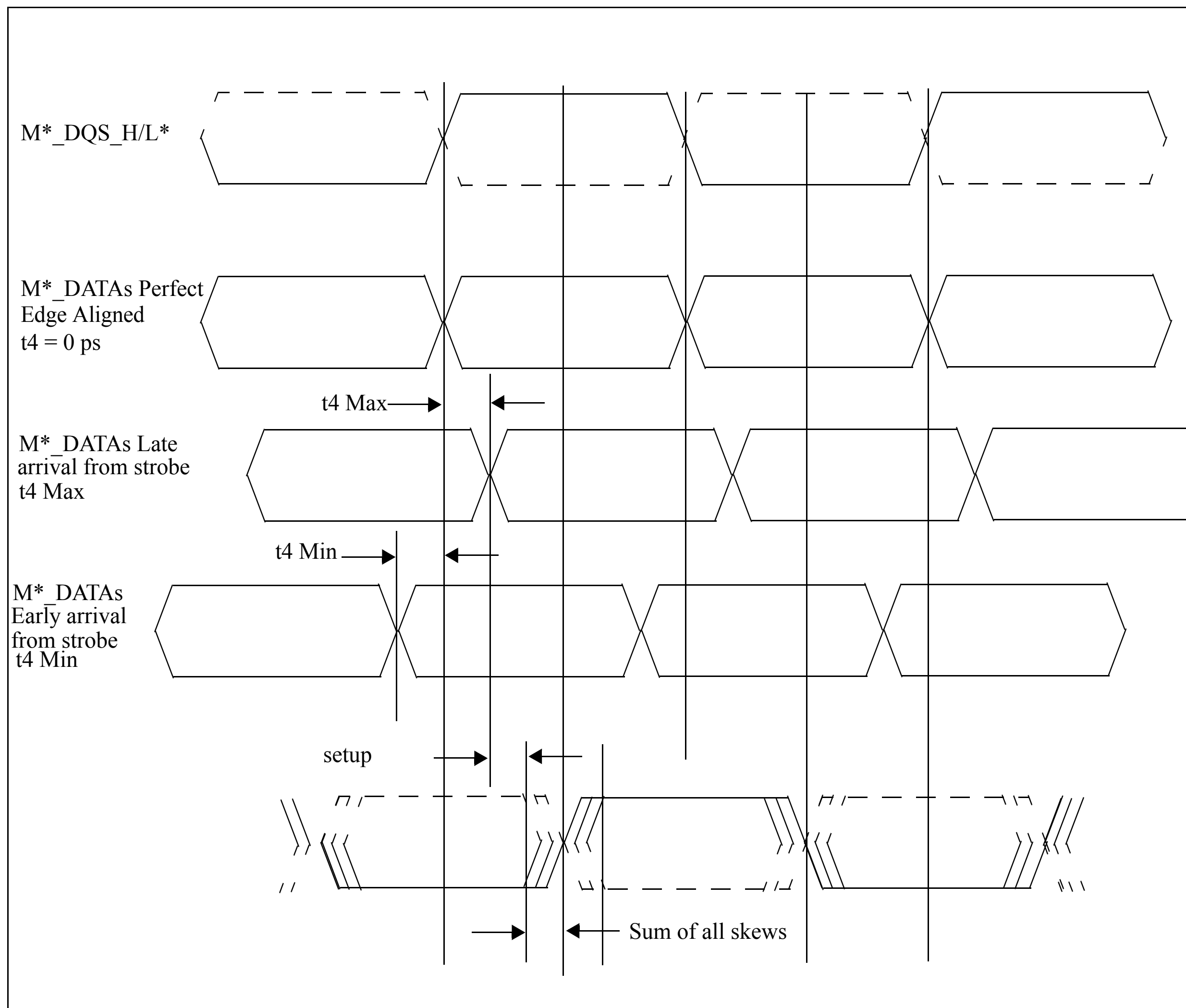

Figure 10. The t4 Timing Parameter

17. *The slow operation of 10-ns cycle time is specifically included for functional test purpose only. All electrical characterization is performed at full speed; however, all functional tests are performed at 10-ns cycle time.*
18. *This parameter is intended to give guidance for DRAM data bus simulation. It cannot be tested on a tester. It is guaranteed by design.*

3.3 DDR2 SDRAM Output Pin States during Reset, S1, and S3

The default pin states for DDR2 SDRAM output pins during reset and ACPI power management states are listed in Table 18. Chapter 7, on page 38, contains additional information and requirements for signal sequencing for certain input and output pins.

Table 18. DDR2 SDRAM Output Pin States During Reset, S1, and S3†

Pin Name	Reset	S1	S3	Comments
M*_CLK_*	0	Z	Z	Tristated in S1 only under AltVid and only if programmed to do so.
M*_DQS_*	Z	Z	Z	
M*_CKE*	0	0	0	
M*_DATA*	Z	Z	Z	
M*_CHECK*	Z	Z	Z	
M*_ERR*	X	X	X	
M*_PAR*	0	Z	Z	
M*_CS_L*	0	Z	Z	
M*_ODT*	0	Z	Z	
M*_RAS_L	0	Z	Z	
M*_CAS_L	0	Z	Z	
M*_WE_L	0	Z	Z	
M*_ADD*	0	Z	Z	
M*_BANK*	0	Z	Z	
M*_RESET_L	0	0	0	In S3, M*_RESET_L is forced to Logic 0.
M_ZN	0	0	Z	
M_ZP	1	1	Z	

†Notes:

- *For differential pins “0” and “1” refer to the high-end differential output. Low-end differential outputs are inverted.*
- *Definition of pin states:*
  - *X—Either logic 1 or logic 0.*
  - *Z—Tristated.*
  - *T—Toggling between 0 and 1.*

4 Miscellaneous Pins

4.1 CLKIN_H/L Pins

Table 19. Operating Conditions for CLKIN_H/L

Symbol	Parameter	Unit	Min	Typ	Max	Notes
V_{IH}	Input high voltage	mV			VDDIO + 150	1
V_{IL}	Input low voltage	mV	0			1
V_{ICM}	Input common mode voltage	mV	700		1100	3
Delta V_{CROSS}	Change in crossover point voltage over all edges	mV			400	4
F	Input frequency range	MHz	198.8		200	
ppm	Long term accuracy	ppm	–300		300	5
S_{FALL}	Input falling edge slew rate	V/ns	–10		–1.2	2,6
S_{RISE}	Input rising edge slew rate	V/ns	1.2		10	2,6
T_{JC}	Jitter, cycle-to-cycle	ps	0		200	7
VID	Differential input voltage	mV	250			8
Delta VID	Change in VID_dc cycle-to-cycle	mV	–150		150	9
C_{IN}	Input capacitance	pF	0		3	2
DC	Duty cycle	%	30		70	10

Notes:
1.Single-ended measurement using absolute voltages. Refer to Figure 11 on page 29.
2.Only simulated at the receive die pad. This parameter is intended to give guidance for simulation. It is guaranteed by design and cannot be tested on a tester.
3.Single-ended measurement using mathematical function (average voltage of CLKIN_H and CLKIN_L).
4.Single-ended measurement at crossover point. Value is max - min over all time. Refer to Figure 11 on page 29.
5.Measured with spread spectrum turned off.
6.Differential measurement through the range of ±250 mV. Refer to Figure 11 on page 29.
7.Maximum difference of t_{CYCLE} between any two adjacent cycles.
8.Magnitude of differential measurement. Refer to Figure 11 on page 29.
9.The difference in magnitude of two adjacent VID_dc measurements.
10.Defined as t_{HIGH} / t_{CYCLE}. Refer to Figure 11 on page 29.

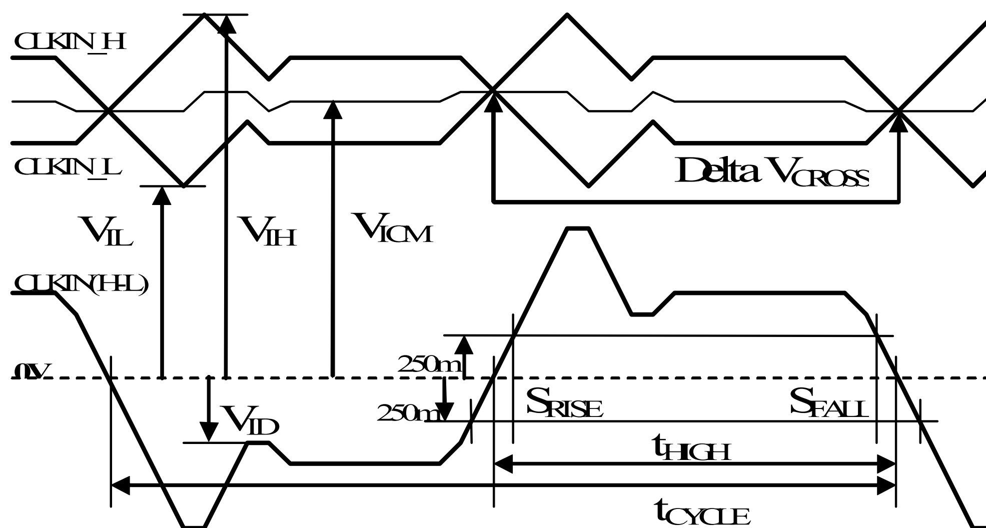

Figure 11. CLKIN_H/L Waveform Diagram

4.2 VID Interface Pins

Table 20. Combined AC and DC Operating Conditions for VID[5:0], and PSI_L

Symbol	Parameter	Unit	Min	Typ	Max	Notes
VOH	Output high voltage (logic 1) @ IOH = 5 mA	V	0.83 * VDDIO		VDDIO	
VOL	Output low voltage (logic 0) @ IOL = –5 mA	V	VSS		0.18 * VDDIO	
IOH	Output high current (V_{OUT} = Min VOH)	mA	5			
IOL	Output low current (V_{OUT} = Max VOL)	mA			–5	
IOZ	Output leakage current	mA	–1		1	
SOUT	Output slew rate	V/ns	1		10	

4.3 Miscellaneous Input Pins

Table 21. Combined AC and DC Operating Conditions for RESET_L, LDTSTOP_L, and PWROK

Symbol	Parameter	Unit	Min	Typ	Max	Notes
VIH	Input high voltage (logic 1)	mV	0.58 * VDDIO		VDDIO	
VIL	Input low voltage (logic 0)	mV	VSS		0.42 * VDDIO	
IL	Input leakage current	mA	–1		1	
CIN	Input capacitance	pF			4	
SIN	Input slew rate	V/ns	0.01			1

Notes:

1.Minimum input slew rate specification is based on HyperTransport™ technology input minimum slew rate specification for single-ended signals.

Table 22. Combined AC and DC Operating Conditions for TCK, TDI, TMS, TRST_L, and DBREQ_L

Symbol	Parameter	Unit	Min	Typ	Max	Notes
VIH	Input high voltage (logic 1)	mV	0.66 * VDDIO		VDDIO	
VIL	Input low voltage (logic 0)	mV	VSS		0.34 * VDDIO	
IL	Input leakage current	mA	–1		1	
CIN	Input capacitance	pF			4	
SIN	Input slew rate	V/ns	0.50			

4.4 Miscellaneous Output Pins

Table 23. Combined AC and DC Operating Conditions for TDO, DBRDY

Symbol	Parameter	Unit	Min	Typ	Max	Notes
VOH	Output high voltage (logic 1) @ IOH = 4.2 mA	mV	0.83 * VDDIO		VDDIO	
VOL	Output low voltage (logic 0) @ IOl = –4.2 mA	mV	VSS		0.18 * VDDIO	
IOH	Output high current (V_{OUT} = Min VOH)	mA	4.2			
IOL	Output low current (V_{OUT} = Max VOL)	mA			–4.2	
IOZ	Output leakage current	mA	–1		1	
SOUT	Output slew rate	V/ns	1		10	

Table 24. Combined AC and DC Operating Conditions for THERMTRIP_L

Symbol	Parameter	Unit	Min	Typ	Max	Notes
VOL	Output low voltage (logic 0) @ IOL = –5 mA	mV	VSS		0.18 * VDDIO	
IOZ	Output leakage current	mA	–1		1	
IOL	Output low current (V_{OUT} = Max VOL)	mA			–5	
SOUT	Output slew rate	V/ns	See Note 1			

Notes:
1.Slew rates for open-drain signals are pullup-dependent.

4.5 Miscellaneous Bi-Directional Pins

Table 25. Combined AC and DC Operating Conditions for PROCHOT_L

Symbol	Parameter	Unit	Min	Typ	Max	Notes
VIH	Input high voltage (logic 1)	mV	0.66 * VDDIO		VDDIO	
VIL	Input low voltage (logic 0)	mV	VSS		0.34 * VDDIO	
VOL	Output low voltage (logic 0)	mV	VSS		0.18 * VDDIO	
SIN	Input slew rate	V/ns	See Note 1.			
SOUT	Output slew rate	V/ns	See Note 1.			

Notes:
1.Slew rates for open-drain signals are pullup-dependent.

4.6 Miscellaneous Pin States During Reset and Power Management States

Table 26. Miscellaneous Output Pin States During Reset, S1, and S3†

Pin Name	Reset	S1	S3	Comments
SID	X	X	Z	
VID*	X	X	X	
PSI_L	X	X	Z	
TDO	X	X	Z	
DBRDY	0	0	Z	
THERMTRIP_L	Z	X	Z	
PROCHOT_L	X	X	Z	

†Notes:
- *For differential pins “0” and “1” refer to the high-end differential output. Low-end differential outputs are inverted.*
- *Definition of pin states:*
  - *X—Either logic 1 or logic 0.*
  - *Z—Tristated.*
  - *T—Toggling between 0 and 1.*

Table 27. Miscellaneous Input Pin Requirements During Reset, S1, and S3†

Pin Name	Reset	S1	S3	Comments
PWROK	Refer to Section 7.1 on page 38	1	0	
RESET_L	Refer to Section 7.1 on page 38	1	0	
LDTSTOP_L	Refer to Section 7.1 on page 38	0	X	

†Note:
- *Definition of pin states:*
  - *X—Either logic 1 or logic 0.*
  - *Z—Tristated.*
  - *T—Toggling between 0 and 1.*

5 Thermal Diode and Thermal Protection

An on-die thermal diode is provided as a tool for thermal management. An external thermal monitor is necessary to measure the temperature of the thermal diode.

5.1 Thermal Diode Specifications

The specifications for on-die thermal diode for socket F (1207) processors and socket AM2 processors with a lidded package are different from the specifications for socket S1g1 processors with a lidless package as tabulated in the following tables. Refer to the following documents for functional and mechanical details.

- *Socket F (1207) Processor Functional Data Sheet*, order #31118, for socket F (1207) processors.
- *Socket AM2 Processor Functional Data Sheet*, order #31117, for socket AM2 processors.
- *Socket S1g1 Processor Functional Data Sheet*, order #31731, for socket S1g1 processors.

Table 28. Thermal Diode Specifications for Socket F (1207) and Socket AM2 Processors

Symbol	Parameter	Units	Min	Typ	Max	Notes
$I_{diode_lidded_pckg}$	Thermal diode sourcing current for processors with lidded package	µA	5		250	1, 2
$T_{Offset_lidded_pckg}$	Thermal diode temperature offset for processors with lidded package	ºC	–52		10	3, 4, 5, 6

Notes:

1.Thermal diode sourcing current should always be used in forward bias.

2.T_{Offset} supports diode thermal monitor using two sourcing currents only. AMD does not support other sourcing current implementations.

3.T_{Offset} is used to normalize the diode thermal monitor reading to the Tcontrol scale. T_{Offset} should be added to the diode thermal monitor reading.

$T_{control}$ = diode thermal monitor reading +T_{Offset} .

System thermal policy should ensure that Tcontrol_max is not exceeded. Tcontrol_max is specified in the appropriate power and thermal data sheet.

4.Thermal solutions should not be designed and validated using the thermal diode. Thermal solutions should be designed and validated against the case temperature specification per the methodology documented in the appropriate processor thermal design guide.

5.T_{Offset} is unique for each processor and is programmed at the factory. T_{Offset} value is found in the Thermtrip Status Register described in the BIOS and Kernel Developer's Guide for AMD NPT Family 0Fh Processors, *order# 32559.*

6.If the diode thermal monitor has an ideality factor different from 1.008, a small correction to this offset is required. Contact your diode thermal monitor vendor to determine if additional correction is required.

Table 29. Thermal Diode Specifications for Socket S1g1 Processors

Symbol	Parameter	Units	Min	Typ	Max	Notes
$I_{diode_lidless_pckg}$	Thermal diode sourcing current for processors with lidless package	µA	5		250	1, 2
$T_{Offset_lidless_pckg}$	Thermal diode temperature offset for processors lidless package	°C	–32		0	3, 4, 5

Notes:

1.Thermal diode sourcing current should always be used in forward bias.

2.T_{Offset} *supports diode thermal monitor using two sourcing currents only. AMD does not support other sourcing current implementations.*

3.T_{Offset} *should be added to the diode thermal monitor reading.*

T_{diode} *= diode thermal monitor reading +*T_{Offset} *.*

4.T_{Offset} *is unique for each processor and is programmed at the factory.* T_{Offset} *value is found in the Thermtrip Status Register described in the* BIOS and Kernel Developer's Guide for AMD NPT Family 0Fh Processors, *order# 32559.*

5.If the diode thermal monitor has an ideality factor different from 1.008, a small correction to this offset is required. Contact your diode thermal monitor vendor to determine if additional correction is required.

5.2 THERMTRIP_L Thermal Protection

This section describes the parameters relating to thermal protection. THERMTRIP functionality is a hardware failsafe mechanism to protect the processor from thermal damage. When a factory determined thermal shutdown temperature, $T_{SHUTDOWN}$, is reached, the processor asserts the THERMTRIP_L signal. Upon sensing the assertion of THERMTRIP_L signal, the motherboard must shut down the voltage on VDD within the specific delay, T_{SD_DELAY} , to prevent thermal damage to the processor.

Thermal protection circuitry reference designs and thermal solution guidelines could be found in the following documents:

- *Socket S1g1 Motherboard Design Guide*, order# 33164
- *Socket AM2 Motherboard Design Guide*, order# 33165
- *Socket F (1207) Motherboard Design Guide*, order# 33166

Table 30 provides the thermal limits that are necessary to protect the processor from thermal damage.

Table 30. Platform Thermal Protection Limits for the Processor

Symbol	Parameter Description	Max	Units	Notes
$T_{SHUTDOWN}$	THERMTRIP shutdown temperature	125	ºC	1
T_{SD_DELAY}	Maximum allowed time from $T_{SHUTDOWN}$ detection to VDD shutdown to prevent thermal damage to the processor	500	ms	2

Notes:
1.THERMTRIP uses an internal temperature sensor independent of the thermal diode.
2.VDD shutdown is specified within this context as ramping down of the VDD voltage level to 20% of the nominal VDD level at the maximum performance state.

6 Power Supplies

6.1 Power Supply and PWROK Relationships

Power supply relationships during power-up, powerdown, and entry and exit of any power management state must be controlled in order to ensure proper operation of the device. Power supplies are arranged into power sequencing groups as shown in Table 31. There are no sequencing requirements between power supplies in the same power sequencing group unless specifically noted. The following sections define the sequencing requirements between the power sequencing groups and their relationship to PWROK. These relationships should be specifically ensured by system power generation and distribution schemes. Chapter 7, on page 38, defines additional signal sequencing requirements for power-up, power-down, and entry and exit of power management states.

Table 31. Power Sequencing Group Definitions

Power Group A	Power Group B	Power Group C
VDDIO[1]	VDD	VLDT
VTT[1]		
VDDA		

Notes:
1.VDDIO must never exceed VTT by greater than 1.10 V. This relationship must be enforced at all times including power-up, powerdown, and power failure.

6.2 PWROK Sequencing Requirements

The following bulleted list shows PWROK sequencing requirements.

- All power supplies in all Power Sequencing Groups must be stable and within specification before the assertion of PWROK. Additional power-up sequencing requirements for PWROK are defined and illustrated in Section 7 on page 38.
- PWROK must be deasserted when any supply in any Power Sequencing Group is out of specification.

6.3 Power-Up (S3/S4/S5/G2 Exit) Power Sequencing Group Requirements

The following bulleted list shows power-up (S3/S4/S5/G2) power sequencing group requirements.

- Any special relationships noted within a Power Sequencing Group must be maintained at all times (see Table 31).
- All power supplies in Power Sequencing Group A must be stable and within specification before any power supply in Power Sequencing Group B is greater than 10% of its specified typical operating value.
- All power supplies in Power Sequencing Group B must be stable and within specification before any power supply in Power Sequencing Group C is greater than 10% of its specified typical operating value.

6.4 Powerdown (S4/S5/G2 Entry) and Power Failure (G3 Entry) Power Sequencing Group Requirements

Any special relationships noted within a Power Sequencing Group must be maintained at all times (see Table 31 on page 36). No sequencing relationships are required between the Power Sequencing Groups during powerdown, Power Failure, or S3 entry.

6.5 S3 Entry Power Sequencing Group Requirements

Any special relationships noted within a Power Sequencing Group must be maintained at all times (see Table 31 on page 36). No sequencing relationships are required between the Power Sequencing Groups during powerdown, Power Failure, or S3 entry. DDR2-compatible processors require VDDIO and VTT to remain powered and within specification during S3. All other processor power supply planes are powered down during S3.

7 Signal Sequencing

Figure 12 on page 39 illustrates the signal and power supply sequencing requirements during a cold reset (power-up conditions). The HyperTransport™ link reset sequencing is defined in the *HyperTransport™ I/O Link Specification*. Table 31 on page 36 and Section 6.3 on page 36 define the Power Sequencing Groups and sequencing requirements specific to all system power supplies.

7.1 Power-Up Power Supply and Signal Sequencing

The following numbered group shows power-up power supply and signal sequencing.

1. All power supplies in Power Sequencing Group A (defined in Table 31 on page 36) must be within specification before any supply in Power Sequencing Group B (defined in Table 31) is greater than 10% of its specified typical operating value. Additional power up sequencing requirements for Power Sequencing Group A are noted in Table 31.
2. All power supplies in Power Sequencing Group B (defined in Table 31 on page 36) must be within specification before any supply in Power Sequencing Group C (defined in Table 31) is greater than 10% of its specified typical operating value.
3. RESET_L must be asserted a minimum of 1 ms prior to the assertion of PWROK, as defined in the *HyperTransport™ I/O Link Specification*. CLKIN_H/L must be within specification a minimum of 1 ms prior to the assertion of PWROK.
4. If the JTAG interface is used in a system, the TMS pin must be asserted a minimum of 10 nS before PWROK assertion or TRST_L de-assertion and must be held in the High state a minimum of 10 nS after the assertion of PWROK or TRST_L de-assertion .
5. PWROK remains deasserted at least 1 ms after both CLKIN_H/L and all voltages to the processor are within specification for operation.
6. After PWROK assertion the VID[5:0] signals change from the Metal Mask VID to the value programmed during device manufacturing.
7. LDTSTOP_L must be deasserted a minimum of 1 µs before the deassertion of RESET_L, as defined by the *HyperTransport™ I/O Link Specification*.
8. RESET_L must remain asserted until the clocks from the transmitters of all HyperTransport devices are stable, and a minimum of 1 ms after PWROK assertion as defined in the *HyperTransport™ I/O Link Specification*.

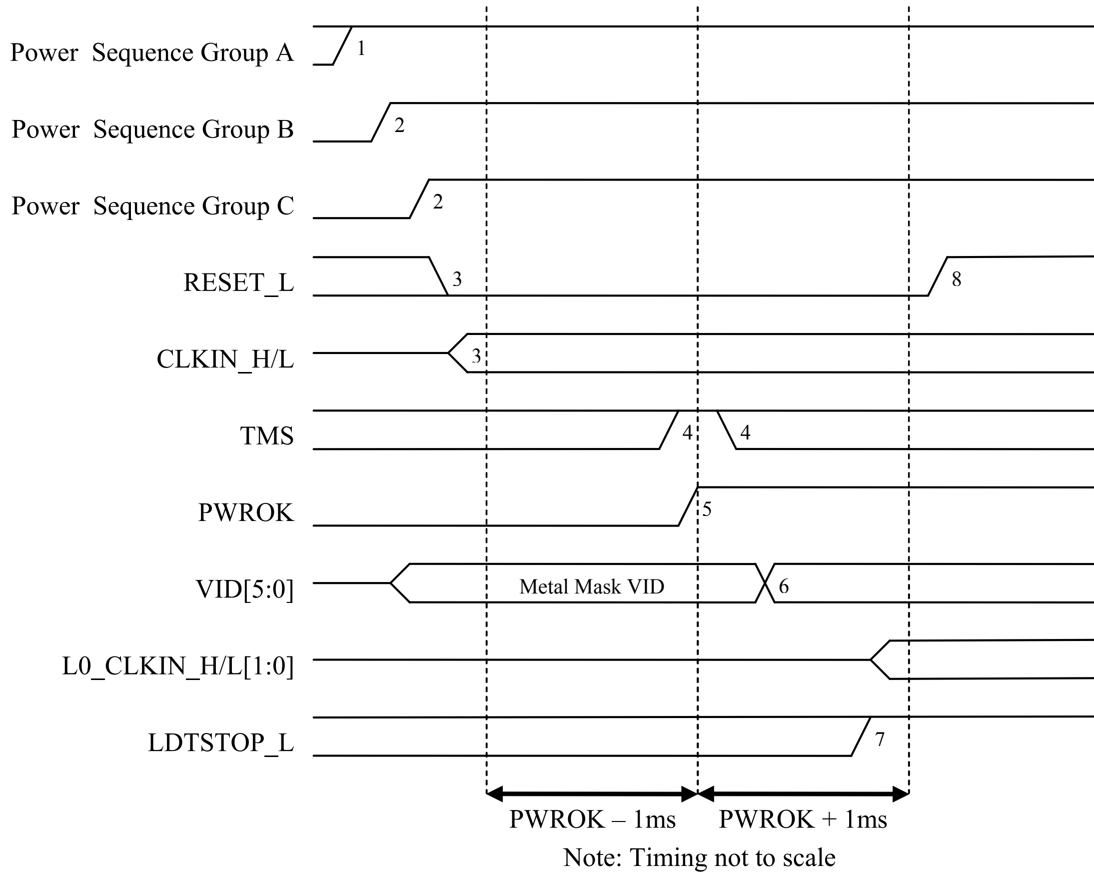

Figure 12. Power-Up Power Supply and Signal Sequencing

8 Internal Termination Reference Information

Table 32 shows internal termination for miscellaneous pins interface and test pins.

Table 32. Internal Termination for Miscellaneous Pins Interface and Test Pins

Pin	Internal Termination	Min Value	Max Value
TCK	Pullup to VDDIO [1]	460 ohms	730 ohms
TMS	Pullup to VDDIO [1]	460 ohms	730 ohms
TRST_L	Pullup to VDDIO [1]	460 ohms	730 ohms
TDI	Pullup to VDDIO [1]	460 ohms	730 ohms
DBREQ_L	Pullup to VDDIO [1]	460 ohms	730 ohms
TEST26	Pullup to VDDIO [1]	460 ohms	730 ohms
TEST27	Pullup to VDDIO [1]	460 ohms	730 ohms
TEST24	Pulldown to VSS [1]	460 ohms	730 ohms
TEST20	Pulldown to VSS [1]	460 ohms	730 ohms
TEST21	Pulldown to VSS [1]	460 ohms	730 ohms
TEST22	Pulldown to VSS [1]	460 ohms	730 ohms
TEST12	Pulldown to VSS [1]	460 ohms	730 ohms
TEST18	Pulldown to VSS [1]	460 ohms	730 ohms
TEST19	Pulldown to VSS [1]	460 ohms	730 ohms

Notes:

1.Systems that do not require use of these pins can rely on the internal termination to pull the signals to the proper inactive state. When these pins are used, they must not be driven with open-drain outputs, otherwise additional termination is required.